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Development of Middle Size Full In-Cell LCD Module for PC with IGZO

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Abstract

We developed the world's first middle size full in-cell LCD for PC with IGZO technology. We evaluated a new Gate driver In Panel (GIP) structure with latch circuit and confirmed that there were no problems with display and touch panel (TP) performance. Furthermore, we did a feasibility study of higher display resolutions and larger size panels, which showed future possibilities.

Author Keywords

Touch Panel; In-Cell; IGZO; GIP; LCD.

1. Introduction

Displays with touch panels have become important for various mobile devices from the view point of operability. Touch panels make it easy to operate smartphones, tablets, PCs and other information terminals.

In the case of LCD modules for PC, the out-cell type film TPs that have long been used lose the merits of a thin LCD module unit and the narrow border of the IGZO panel [1]. For this reason, we aimed to develop a full in-cell model with IGZO technology.

For the in-cell type touch panel technology, micro-switch [4], capacitance [5-6] and optical sensors [7-8] have been proposed, but from the viewpoint of manufacturing problems (yield rate) and the availability of a drive system (touch controller IC), the mainstream of development is a capacitive type.

The essence of the electrostatic capacity in-cell touch technology is how to design a low-load electrode to form a touch electrode in the panel, and how to efficiently synchronize the display drive and the touch panel drive.

In this paper, we report about the development of a middle size full in-cell LCD for PC with IGZO technology and discuss in detail a newly developed IGZO-compatible GIP circuit that is indispensable for providing a pause period during the driving period of the LCD.

2. Prototype

Panel Design: For the full in-cell panel process, the structure in Fig. 1 was adopted. The common ITO was divided into more than 4000 segments for use as TP electrodes. The thickness of TP metal line and insulator layer are key factors for improving TP performance. We designed an equivalent circuit for simulation and set parameters by calculating the time constant for realizing a drive frequency of 100 kHz or greater.

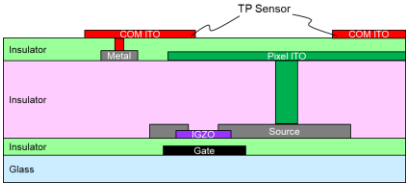

Figure 1. Cross-sectional view of in-cell panel

Table 1. Outline of developed model

Item	Outline
Size	13.3 inch
Display Resolution	FHD (1920 x RGB x 1080 pixels)
Pixel Pitch	166ppi (51.0um x RGB x 153.0um)
Border	Left/Right/Top:1.9mm, Bottom:7.8mm
TP segment number	84(H)x48(H)
Touch method	Full In-Cell (Self-sensing method)
TP pitch	3.5mm x 3.4mm

Driving Scheme: Fig. 2 shows a relationship between the pixel writing period and the TP sensing period in one frame. As shown in Fig. 2, a single frame is divided into a plurality of pixel writing periods and TP sensing periods, so displaying and sensing can be simultaneously performed within one frame by alternately driving the two.

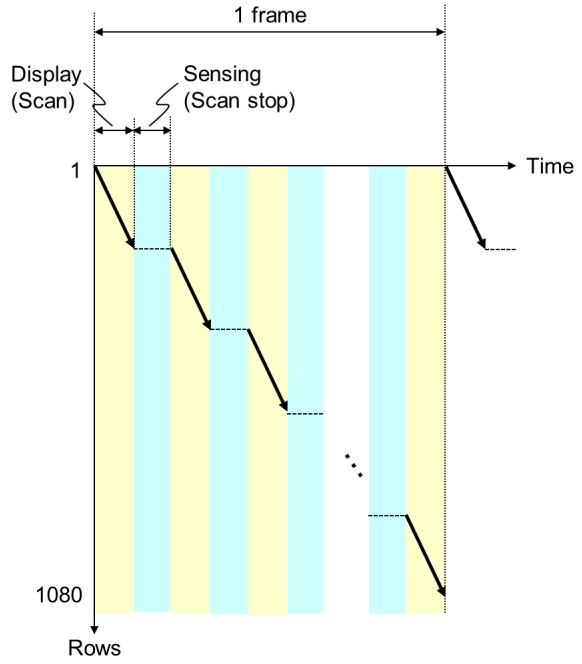

Figure 2. Display and touch sensing timing

3. GIP Circuit

In the sensing period, it is necessary to pause gate scanning and pixel writing. A gate bus line must hold the Low state during the sensing period and scanning must resume after the sensing period. In order to realize these functions, a gate driver (GIP) that does not cause improper operation while gate scanning is stopped is required. We developed new type of gate driver capable of latching the potential in the circuit using IGZO-TFT. Fig. 3 (a) shows a conventional GIP circuit, while Fig. 3 (b) is the GIP circuits developed this time. Fig. 4 shows their respective timing diagrams.

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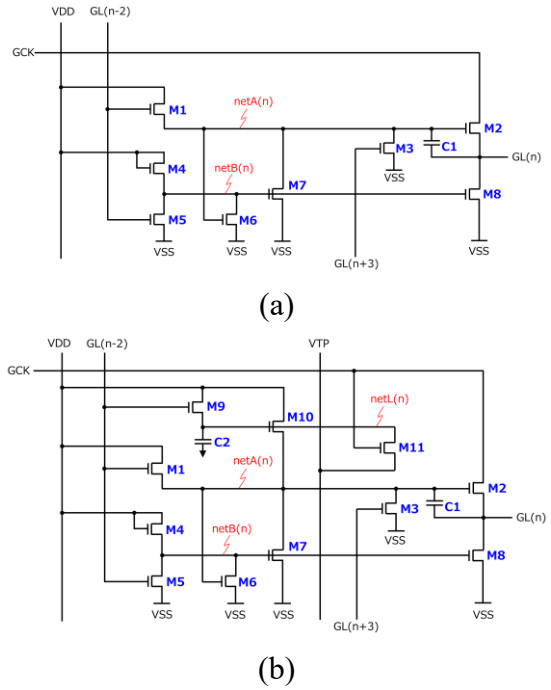


Figure 3. Schematic diagram (a) Conventional GIP (b) GIP with latch function

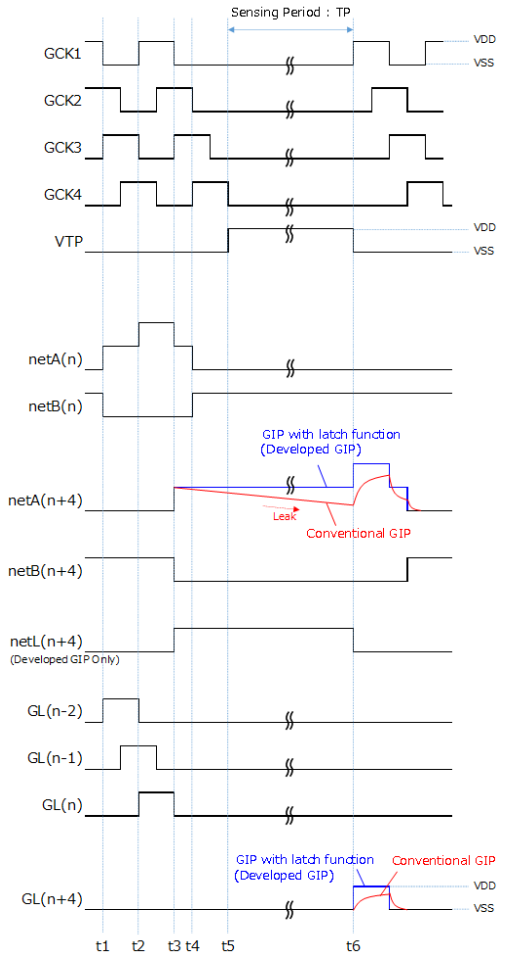


Figure 4. Timing diagram

Conventional GIP: GIP operation will be described with reference to Figs. 3 (a) and 4. First, the GL (n-2) signal ([n-2]th signal of the gate bus-line) is input at time t1, and the netA(n) node is pre-charged via M1. Next, GCK changes from VSS to VDD at time t2, whereby netA(n) is boosted via C1 and GL (n) is charged to VDD via M2. After that, GCK1 changes from VDD to VSS at time t3, whereby GL (n) is discharged from VDD to VSS. At the time t4, since GL (n+3) changes from VSS to VDD, netA (n) is discharged to VSS via M3, and the gate driver operation of the nth line is completed. Here, netB(n) plays the role of a stabilizing circuit (stabilizer) to keep netA(n) and GL(n) at VSS during the unselected period.

After scanning to the (n+3) row, a sensing period is provided from time t5 to time t6. During the sensing period (TP in Fig. 4), GCK is fixed to VSS and gate scanning is paused. In order to resume the gate scan after the sensing period, it is necessary to hold the potential of the pre-charged netA (n+4) during the sensing period.

At this time, voltages Vgs = 0 V and Vds = VA - VSS (VA is the potential of netA) are applied to M3 and M7, and OFF-state leakage currents flow. However, when the TFT characteristics reach the depletion mode (Vth < 0V) due to process variations, a large amount of leakage current flows and the potential of netA (n+4) gradually decreases through M3 and M7 due to the OFF-state leakage current. As a result, netA (n+4) cannot be boosted sufficiently when resuming the gate scanning operation, and GL (n + 4) cannot be charged to VDD. Accordingly, the charge in the pixels in (n+4)th row becomes insufficient and irregular lines that degrade the display quality appear. Since this phenomenon occurs every sensing period, a plurality of irregularities along the gate line appear at regular intervals. Therefore, it is difficult to provide a long latch period in the conventional circuit. On the other hand, the GIP with latch circuit (Fig. 3 [b]) was developed to solve these problems.

Developed GIP: In the GIP circuit, as shown in Fig. 3 (b), a latch circuit composed of the TFTs M9, M10, and M11, the capacitor C2, and the signal VTP is added as compared with the conventional circuit. Fig. 5 shows the flow of charges during the sensing period. The internal node netL(n+4) of the latch circuit is pre-charged by GL (n+2) at time t1, and keeps M10 in the ON state. Since the charge continues from VDD to netA (n+4) via M10, it is possible to re-fill the charge outflowed from netA by the OFF-state leakage current in M2 and M7. As a result, the potential of netA (n+4) can be held, and the gate scan can be resumed properly.

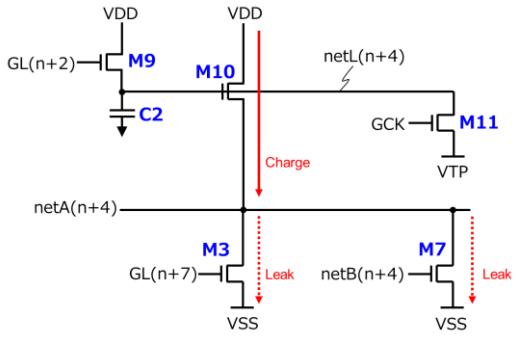


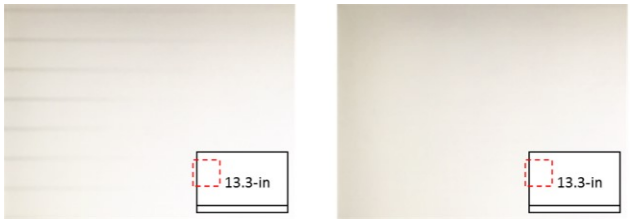
Figure 5. Latch mechanism of developed GIP circuit

4. Results and Discussion

Visible Irregularities: Table 2 shows the results of evaluating the visibility of irregularities for each sensing period in prototype panels using the conventional GIP and developed GIP. When the sensing period is short (250μs), irregularities are not visually recognized in both of the circuits. On the other hand, when the sensing period is expanded to 500μs or 750μs, irregularities are visually recognized along the gate lines in the conventional GIP. However, irregularities are still not visible in GIP with latch function. Fig. 6 shows enlarged views of photographs near the gate driver of each trial panel equipped with conventional GIP, GIP with latch function. In this way, a GIP with latch function can operate properly even during long sensing periods.

Table 2. Visibility of irregularities

Sensing Period	Conventional GIP	GIP with Latch Function
250us	Invisible	Invisible
500us	Visible	Invisible
750us	Visible	Invisible



(a) Conventional GIP (b) GIP with latch function

Figure 6. Visibility of irregularities (Sensing period 750us)

Power Consumption: The measurement results of the power consumption of each GIP are shown in Table 3. The GIP with latch function shows a no increase in power consumption as compared with the conventional circuit.

Table 3. Power consumption of GIP

Conventional GIP	GIP with Latch Function
35.6mW	35.6mW

As described above, we fabricated the GIP with latch functions, realizing higher latch performance than with the conventional GIP. Also, these new GIPs can stop scanning on arbitrary lines. That is, it is possible to freely set the sensing period and timing within one frame. This makes it possible to respond flexibly to various touch panel driving conditions.

Touch Panel Performance: The results of touch performance tests are shown in Table 4. "Linearity", "Jitter" and "Accuracy" were all good at less than 1.0 mm, while SNR=38dB (Cover glass thickness =0.4mm, φ=7mm metal slug). Normally, if the SNR of the touch panel is 35dB or more, operation in a normal environment is performed without any problems. Furthermore, this panel was tuned roughly for an LCD module, therefore SNR might be improved if fine-tuned. Fig.7 shows the developed LCD sample.

Table 4. Results of TP performance tests

Item	Criteria	Result (Φ7mm)
Accuracy	(Center area/Edge area) <1.0mm/<1.5mm	0.72mm/1.25mm
Jitter	(Center area/Edge area) <0.5mm/<0.5mm	0.15mm/0.0mm
Linearity	(Center area/Edge area) <1.0mm/<1.5mm	0.29mm/0.39mm
Multi touch	10 points	10 points
Waterproofness	(a) Water 0.1ml~5ml (touch/ without touch) (b) Mist (touch/ without touch) (c) After swipe the water	OK
Ghost noise	Multi touch on same line	OK
Finger separation	<10mm	10mm

Figure 7. Developed Sample

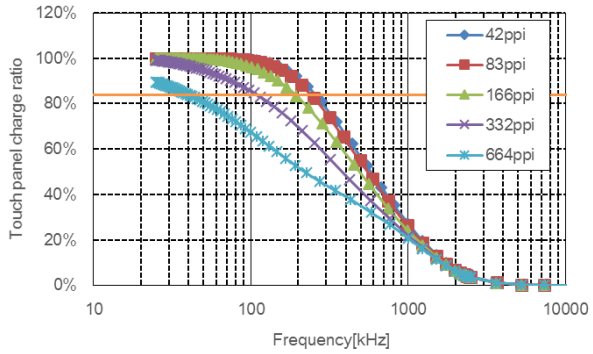
Simulation of the Display Resolution and Panel Size: We simulated the charge ratio vs. the driving frequency by changing the resolution at the maximum load segment (Fig. 8). Fig. 9 shows the equivalent circuit that was used for calculating the time constant of the segment. C_{touch} is the additional capacitance of a finger when the n^{th} electrode was touched. C_n is the parasitic capacitance between the own electrode and the other COM electrode. R_n is the resistance per segment. Although it is not shown in Fig. 9, the load capacitance from the pixel wiring line corresponding to the display resolution is added to the n^{th} electrode. In fact, by calculating the charging characteristic at the n^{th} segment based on this equivalent circuit, it is almost approximated by the product of ΣC_n, which adds all the parasitic capacitance hanging from this system, and ΣR_n, which adds all the wiring resistance (Fig. 10).

If the display resolution is increased, the number of cross lines (gate or source lines) at the COM electrode increases, which increases parasitic capacitance and makes quick charging difficult. Our calculation result is that UHD has 1.8 times higher load than FHD.

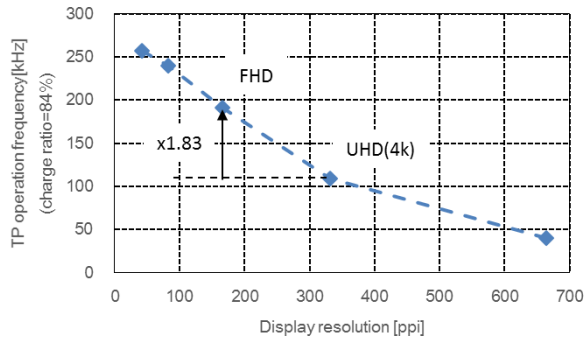
On the other hand, the maximum display size of this full in-cell module is shown in Fig. 11. We define the panel load condition that this prototype 13.3-inch FHD can be operated sufficiently with the finger as "1". Fig. 11 suggests that bigger size panels need a lower panel load. As the display size increases, you can see that the panel load needs to be sharply lowered.

It is confirmed that this load can be achieved by optimizing the thickness of the TP electrode and insulating layer, described in Fig. 1, in this developed panel.

But, this configuration has its limits due to manufacturing restrictions and the influence on the optical characteristics (color change, transmittance decrease, etc.). If a bigger size of panel beyond that is required, a new structure will be necessary to lower the panel load.



(a)



(b)

Figure 8. Display resolution and calculated charge ratio

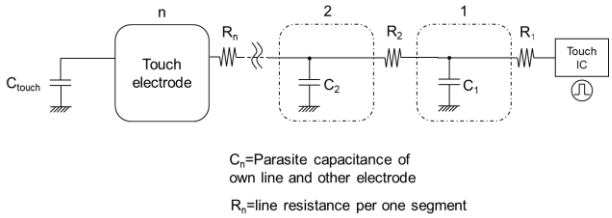


Figure 9. Equivalent circuit for touch time constant simulation

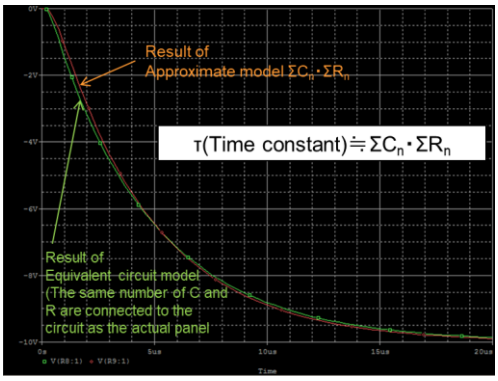


Figure 10. Simulation result of charging curve

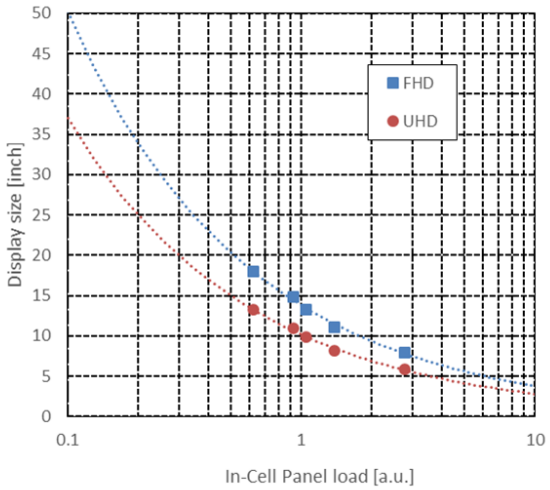


Figure 11. Max. display size vs. Panel load (Panel load reference is 13.3" FHD.)

5. Conclusion

We have developed a 13.3-in FHD full in-cell touch system with IGZO technology by using a new latch circuit. Our system demonstrates superior optical and touch performance.

By installing full in-cell technology on the IGZO panel, it is possible to achieve the same narrow borders and thin modules as a normal panel without TP. So, it will increase the flexibility of PC set design. Even in the middle size panel range, we believe that the technology of the full in-cell touch panel will become a main stream, just like with smartphones.

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